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Term	Documents
(11 AND 18).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	9
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<i>DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>			
<u>L24</u>	L18 and l11	9	<u>L24</u>
<u>L23</u>	L18 and l10	9	<u>L23</u>
<u>L22</u>	L18 and l9	4	<u>L22</u>
<u>L21</u>	L18 and l8	10	<u>L21</u>
<u>L20</u>	L18 and l7	1	<u>L20</u>
<u>L19</u>	L18 and l6	10	<u>L19</u>
<u>L18</u>	l5 and (interfac\$5 or input\$1 or output\$1) near6 (gate\$1 or register\$1)	335	<u>L18</u>
<i>DB=PGPB,USPT; PLUR=YES; OP=OR</i>			
<u>L17</u>	l5 and l11	9	<u>L17</u>
<u>L16</u>	l5 and l10	9	<u>L16</u>
<u>L15</u>	l5 and l9	5	<u>L15</u>

<u>L14</u>	l5 and l8	12	<u>L14</u>
<u>L13</u>	l5 and l7	1	<u>L13</u>
<u>L12</u>	l5 and l6	11	<u>L12</u>
<u>L11</u>	(326/41,114,125)![CCLS]	1503	<u>L11</u>
<u>L10</u>	(326/41,114,125)[CCLS]	1503	<u>L10</u>
<u>L9</u>	(716/18)[CCLS]	948	<u>L9</u>
<u>L8</u>	(716/14-19)[CCLS]	3288	<u>L8</u>
<u>L7</u>	(712/223)[CCLS]	218	<u>L7</u>
<u>L6</u>	(712/2-300)[CCLS]	11741	<u>L6</u>
<i>DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>			
<u>L5</u>	L4 and boolean	424	<u>L5</u>
<u>L4</u>	L3 and short\$3 near4 circuit\$3	4390	<u>L4</u>
<u>L3</u>	(conjunct\$4 or disjunct\$5) and ("AND" or "OR") and (dynamic\$6 or reconfigur\$5)	65263	<u>L3</u>
<i>DB=USPT; PLUR=YES; OP=OR</i>			
<u>L2</u>	L1 and short\$3	1	<u>L2</u>
<u>L1</u>	5682519.pn.	1	<u>L1</u>

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IEEE Conference Proceeding

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**1. A self-organizing binary decision tree for incrementally defined rule-based systems**

Martinez, T.R.; Campbell, D.M.;
Systems, Man and Cybernetics, IEEE Transactions on
Volume 21, Issue 5, Sept.-Oct. 1991 Page(s):1231 - 1238
Digital Object Identifier 10.1109/21.120075

[AbstractPlus](#) | Full Text: [PDF](#)(680 KB) **2. The set-theoretical modification of Boolean functions minimax covering method**

Rytsar, B.; Minziuk, V.;
Modern Problems of Radio Engineering, Telecommunications and Computer Science, 2004. Proce
International Conference
24-28 Feb. 2004 Page(s):46 - 48
Digital Object Identifier 10.1109/TCSET.2004.1365865

[AbstractPlus](#) | Full Text: [PDF](#)(325 KB) **3. Some peculiarities of the designed logical circuit optimization**

Shipunov, V.; Razumov, P.A.; Kuptsov, E.O.;
Modern Techniques and Technologies, 2003. MTT 2003. Proceedings of the 9th International Scie
Conference of Students, Post-graduates and Young Scientists
7-11 April 2003 Page(s):216 - 218

[AbstractPlus](#) | Full Text: [PDF](#)(342 KB) **4. Improving response time of programmable logic controllers by use of a Boolean coprocessor**

Donandt, J.;
CompEuro '89., 'VLSI and Computer Peripherals. VLSI and Microelectronic Applications in Intellige
their Interconnection Networks', Proceedings.
8-12 May 1989 Page(s):4/167 - 4/169
Digital Object Identifier 10.1109/CMPEUR.1989.93466

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